11-16-00

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JC957 U.S. PTO
11/15/00

Attorney Docket No. SAM-169
PATENT

JC675 U.S. PTO
09/714325
11/15/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): Sung-Bae Park

For (title): BRANCH PREDICTION METHOD USING ADDRESS TRACE

CERTIFICATE OF MAILING
37 C.F.R. § 1.10

"Express Mail" Mailing Label Number EL681163189US
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, DC 20231.

Date: 11/15/00 Lizabeth M Sumner
Lizabeth M. Sumner
Lizabeth M Sumner
Print Name

1. **Type of Application** This new application is for a(n)

☒ Original (nonprovisional)
☐ Design
☐ Plant
☐ Divisional.
☐ Continuation.
☐ Continuation-in-part (C-I-P).

2. **Benefit of Prior Application(s)**

☒ The new application being transmitted claims the benefit of prior Korean application(s) no. 99-50627 See item 7 .

3. **Papers Enclosed**

7 Pages of specification

1 Pages of claims

1 Page of Abstract

5 Sheets of drawings
☒ formal
☐ informal

____ Page of Cover Sheet

☐ The **enclosed** drawing(s) are photograph(s), and there is also attached a "PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)." 37 C.F.R. 1.84(b).

4. Additional papers enclosed

- ☐ Preliminary Amendment
- ☐ Information Disclosure Statement (37 C.F.R. 1.98)
- ☐ Form PTO-1449 (PTO/SB/08A and 08B)
- ☐ Copies of cited references
- ☐ Declaration of Biological Deposit
- ☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleoticle and/or amino acid sequence.
- ☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative
- ☐ Special Comments
- ☒ Other: Return Postcard.

5. Declaration or oath

- ☒ Enclosed
  - ☐ Unexecuted
  - ☒ Executed by
    - ☒ inventors
    - ☐ legal representative of inventor(s). 37 CFR 1.42 or 1.43.
    - ☐ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.
    - ☐ This is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. See item 12 below for fee.
- ☐ Not Enclosed

- ☐ Application is made by a person authorized under 37 C.F.R. 1.41 (c) on behalf of all the above named inventor(s).
    - ☐ Showing that the filing is authorized.

6. Assignment

- ☒ An assignment of the invention to Samsung Electronics Co., Ltd.
  - ☒ is attached. A separate ☐ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☒FORM PTO 1595 is also attached. will follow.

7. Certified Copy

Certified copy(ies) of application(s)

Country	Appln. no.	Filed
Korea	99-50627	November 15, 1999

from which priority is claimed

☒ are attached.

☐ will follow.

8. Fee Calculation (37 C.F.R. 1.16)

CLAIMS AS FILED

	Number filed		Number Extra	Rate	Basic Fee 37 C.F.R. 1.16(a) **$710.00**
Total Claims (37 CFR 1.16(c))	4	- 20 =	0	$ 18.00	0
Independent Claims (37 CFR 1.16(b))	1	- 3 =	0	$ 80.00	0
Multiple dependent claim(s), if any (37 CFR 1.16(d))			+	$270.00	

☐ A Preliminary Amendment canceling claims is enclosed. The filing fee is calculated based on the number of claims remaining after entry of the Preliminary Amendment.

☐ Amendment deleting multiple-dependencies is enclosed.

☐ Fee for extra claims is not being paid at this time.

Filing Fee Calculation $ 710.00

9. **Small Entity Statement(s)**

☐ Verified Statement(s) that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is (are) attached.

☐ Status as a small entity was claimed in prior application ______________, filed on________________ from which benefit is being claimed for this application under:

35 U.S.C. ☐ 119(e),
☐ 120,
☐ 121,
☐ 365(c),

and which status as a small entity is still proper and desired.

☐ A copy of the verified statement in the prior application is included.

Filing Fee Calculation (50% of A, B or C above)

$____________

10. **Fee Payment Being Made at This Time**

☐ Not Enclosed

☐ No filing fee is to be paid at this time.
(This and the surcharge required by 3 7 C. F.R. 1.16(e) can be paid subsequently.)

☒ Enclosed

☒ Basic filing fee $ 710.00

☒ Recording assignment
($40.00; 37 C.F.R. 1.21(h))
(See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION".) $ 40.00

Total fees enclosed $ 750.00

11. **Method of Payment of Fees**

☒ Checks in the amounts of $ 710.00, 40.00

☐ Charge Account No. 19-0079 in the amount of $ ________________
A duplicate of this transmittal is attached.

12. Authorization to Charge Additional Fees

☒ The Commissioner is hereby authorized to charge the following additional fees during the entire pendency of this application to Account No. 19-0079.

- ☒ 37 C.F.R. 1.16(a), (f) or (g) (filing fees)
- ☒ 37 C.F.R. 1.16(b), (c) and (d) (presentation of extra claims)
- ☐ 37 C.F.R. 1. 1 6(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)
- ☐ 37 C.F.R. 1.17 (application processing fees)
- ☐ 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

13. Instructions as to Overpayment

☒ Credit Account No. 19-0079

☐ Refund

Respectfully submitted,

Steven M. Mills
Registration Number 36,610
Attorney for Applicant

Date: November 15, 2000

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PATENT
Attorney Docket No. SAM-169

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Sung-Bae Park
Filing Date: Herewith
Title: BRANCH PREDICTION METHOD USING ADDRESS TRACE

CERTIFICATE OF MAILING UNDER 37 C.F.R.§ 1.10

"Express Mail" Mailing Label Number EL681163189US I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, DC 20231.

November 15, 2000
Date

Lizabeth M. Sumner
Lizabeth M. Sumner

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

TRANSMITTAL LETTER

Sir:

Enclosed herewith for filing in the above-identified patent application please find the following listed items:

1. New Application Transmittal;
2. New Patent Application;
3. Executed Declaration, Petition and Power of Attorney;
4. Five (5) Pages of Formal Drawings;
5. Certified copy of Priority Document- Korean Application Number 99-50627;
6. Check in the amount of $710.00 to cover requisite fee;
7. Assignment Recordation Form Cover Sheet - - PTO-1595;
8. Executed Assignment;
9. Check in the amount of $40.00 to cover assignment recordation fee; and
10. Return Postcard.

In connection with the foregoing matter, please charge any additional fees which may be due, or credit any overpayment, to Deposit Account Number 19-0079. A duplicate copy of this letter is provided for this purpose.

Respectfully submitted,

Steven M. Mills

Date: November 15, 2000

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Attorney for Applicant

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BRANCH PREDICTION METHOD USING ADDRESS TRACE

This application relies for priority upon Korean Patent Application No. 1999-50627, filed on November 15, 1999, the contents of which are herein incorporated by reference in their entirety.

Background of the Invention

1. Field of the Invention

The present invention relates to a branch prediction method and, more particularly, to a branch prediction method using an address trace.

2. Description of the Related Art

Fig. 1 shows fourth generation microarchitecture, which is cited from Figure 1 of a paper entitled "Trace Processors: Moving to Fourth Generation Microarchitecture," IEEE Computer, pp. 68-74, September 1997, by James E. Smith & Sriram Vajapeyam. In Fig. 1, (a) is the first generation microarchitecture serial processors which began in the 1940s with the first electronic digital computers and ended in the early 1960s. The serial processors fetch and execute each instruction before going to the next. Diagram (b) is the second generation microarchitecture using pipelining. Such architectures were the norm for high-performance processing until the late 1980s. Diagrams (c) and (d) are the third and fourth generation microarchitectures that are characterized by superscalar processors. The third and fourth generation architectures first appeared in commercially available processors in the late 1980s.

As shown in Fig. 1, high-performance processors of the next generation will be composed of multiple superscalar pipelines, with some higher level control that dispatches groups of instructions to the individual superscalar pipes. The superscalar processors, which can patch a group of instructions to a cache block at the same time and process the instructions in parallel, are afflicted with performance degradation resulting from pipeline stall and abort of missed instruction rather than prediction error. Therefore, correct branch

prediction is very significant to the superscalar processors.

As mentioned above, a critical technology to achieve high performance of superscalar processors is to optimally use pipelines. The most significant design factor is a branch prediction method. A branch predictor operates to predict the outcome of a branch instruction before performing a condition check of the branch instruction based on a predetermined branch prediction approach. A central processing unit (CPU) then fetches the next instruction according to the predicted result. A pipeline technique is adopted to solve a pipeline stall phenomenon that causes performance degradation of a CPU. However, when a branch prediction is missed, many instructions from the incorrect code section may be in various stages of processing in the instruction execution pipeline.

On encountering such a misprediction, instructions following the mispredicted conditional branch instruction in the pipeline are flushed, and instructions from the other, correct code section are fetched. Flushing the pipeline creates bubbles or gaps in the pipeline. Several clock cycles may be required before the next useful instruction completes execution, and before the instruction execution pipeline produces useful output. Such incorrect guesses cause the pipeline to stall until it is refilled with valid instructions, this delay is called the mispredicted branch penalty.

Generally, a processor with 5-step pipelines has a branch penalty of two cycles. For example, in 4-way superscalar design, 8 instructions are subject to loss. If a pipeline is expanded, more instructions are subject to loss and the branch penalty increases. Since programs generally branch in every 4 or 6 instructions, misprediction causes acute performance degradation in a deep pipeline design.

There have been efforts to reduce the above-mentioned branch penalty. Recently, a trace processor using a trace cache has been applied. The trace processor is disclosed in the paper "Trace Processors: Moving to Fourth Generation Microarchitecture," by James E. Smith & Sriram Vajapeyam.

Fig. 2A shows a dynamic sequence of basic blocks embedded in a conventional instruction cache 21. Fig. 2B shows a conventional trace cache 22. Referring now to Fig. 2A, arrows indicate a branch “taken” (jumping to target code section). In the instruction

cache 21, even multiple branch predictions created at every cycle require 4 cycles to fetch instructions in basic blocks “ABCDE” because instructions are stored in discontinuous caches.

Accordingly, some have proposed a specific instruction cache to capture long dynamic instruction sequences. Each line of the specific instruction cache stores a snapshot or trace of a dynamic instruction stream, as shown in Fig. 2B. This cache is referred to as a trace cache 22, which is disclosed in a paper entitled "Expansion Caches for Superscalar Processors," Technical Report CSL-TR-94-630, Stanford Univ., June 1994, by J. Johnson; U. S. Patent No. 5,381,533 entitled "Dynamic Flow Instruction Cache Memory Organized Around Trace Segments Independent Of Virtual Address Line," issued on January 1995 to A. Peleg & U. Weiser; and a paper entitled "Trace Cache: A Low Latency Approach To High Bandwidth Instruction Fetching," Pro. 29th Int’l Symp. Microarchitecture, pp. 24-34, December 1996, by E. Rotenberg, S. Bennett, & J. Smith.

Furthermore, the trace cache 22 is disclosed in a paper entitled "Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing," Proc. 25th Int’l Symp. Computer Architecture, pp. 262-271, June 1998, by Sanjay Jeram Patel, Marius Evers, and Yale N. Patt; a paper entitled "Evaluation of Design Options for the Trace Cache Fetch Mechanism," IEEE TRANSACTION ON COMPUTER, Vol. 48, No. 2, pp. 193-204, February 1999, by Sanjay Jeram Patel, Daniel Holmes Friendly & Yale N. Patt; and a paper entitled "A Trace Cache Microarchitecture and Evaluation," IEEE TRANSACTION ON COMPUTER, Vol. 48, No. 2, pp. 111-120, February 1999, by Eric Rotenberg, Steve Bennett, and James E. Smith.

A dynamic sequence, which is identical to the discontinuous blocks in the instruction cache 21 shown in Fig. 2A, is continuous in the trace cache 22 shown in Fig. 2B. Therefore, instructions stored in the trace cache 22 can sequentially be executed without repeated branch to an address including an instruction according to a conventionally programmed routine. This makes it possible to prevent a branch penalty which occurs in conventional prediction techniques. And, instructions stored in discontinuous positions of the instruction cache 21 are continuously stored in the trace

cache to carry out improved parallel processing.

Because it stores an instruction itself, the trace cache 22 requires decoding to an address corresponding to the instruction. And because the trace cache 22 repeatedly stores even repetitively executed instructions according to their execution order, a chip size of the trace cache 22 increases too much. In order to have enough size to store all instructions, the trace cache 22 inevitably increases in chip size and manufacturing cost.

Summary of the Invention

Therefore, it is an object of the present invention to provide a branch prediction approach using a trace cache, which can shorten address decoding time and decrease chip size and manufacturing cost.

According to the aspect of the present invention, a branch prediction method uses a trace cache. If a routine composed of unrepeated instructions is to be executed, an address corresponding to each instruction in the trace cache according to an order of executed instructions is stored. If a routine composed of repeated instructions is carried out, a routine start address, a routine end address, current access times of the routine, and total access times of the routine are counted and stored.

If the routine composed of the repeated instructions is carried out, the trace cache includes loop counters for counting the current access times and the total current access times. If values of the loop counters are identical to each other, a start address that will be subsequent to the routine is addressed. If the branch prediction is missed, the loop counter is recomposed using the latest updated loop count value.

Brief Description of the Drawings

The foregoing and other objects, features and advantages of the invention will be apparent from the more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

Fig. 1 contains schematic functional block diagrams which illustrate various microarchitectures including fourth-generation microarchitectures.

Fig. 2A is a schematic diagram which shows a dynamic sequence of basic blocks stored in a conventional instruction cache.

Fig. 2B is a schematic diagram which illustrates a conventional trace cache.

Fig. 3 is a schematic diagram which illustrates one example of a repetitive instruction pattern.

Fig. 4 is a schematic diagram which illustrates a pattern where instructions shown in Fig. 3 are stored in a trace cache according to prior art.

Fig. 5 is a schematic diagram which illustrates a structure of an address trace cache according to the present invention.

Fig. 6 is a schematic diagram which illustrates a pattern where instructions shown in Fig. 3 are stored in a trace cache according to the present invention.

Description of Preferred Embodiments of the Invention

A new and improved trace cache stores an address trace itself corresponding to an instruction with a decoded form, thus shortening address decoding time for each instruction. The new and improved trace cache uses a small amount of trace cache memory in storing an address trace to a repetitively executed routine, thus decreasing chip size and manufacturing cost.

Fig. 3 illustrates one example of a repetitive instruction pattern. In a routine 1, operations A and B are repeated 30 times. When the routine 1 is finished, a routine 2 is carried out wherein operations C, D, and E are sequentially repeated 20 times. When the routine 2 is finished, a routine 3 is carried out wherein operations F and G are repeated 40 times.

Assuming that, for example, the routines shown in Fig. 3 are carried out, Fig. 4 shows instructions that are stored in a trace cache 22 according to prior art. Referring now to Fig. 4, the trace cache 22 stores instructions based upon their execution order irrespective of the fact that executed instructions are repeatedly carried out. Accordingly,

the trace cache 22 requires a data storing area for storing 60 instructions (2 instructions x 30 times repetition = 60) for routine 1, a data storing area for storing 60 instructions (3 instructions x 20 times repetition = 60) for routine 2, and a data storing area for storing 80 instructions (2 instructions x 40 times repetition = 80) for routine 3. That is, a total of 200 data storing areas are required for storing instructions for routines 1, 2, and 3 shown in Fig. 3. If 32 bits are required for storing each of the instructions, a data storing area of total 6400 bits (i.e., 800 bytes) is required for routines 1, 2, and 3.

In Fig. 5, in accordance with the invention, an address trace cache 220 is composed of a start address for storing an address where each routine is started, an end address for an address where each routine is finished, an access current loop counter for counting access times of a corresponding routine, and an old access loop counter for indicating total access times of the routine.

For example, if the information of instructions executed in routine 1 is indicated the address trace cache 220, the start address and the end address of routine 1 are stored in the trace cache 220. Then, current access time of routine 1 is stored in the current access loop counter while total access times (e.g., 30 times) of routine 1 is stored in the old access loop counter. As access of the routine is repeated, a value of the current access loop counter is increased. If the value of the current access loop counter is identical to that of the old access loop counter, routine 1 is finished and a start address of routine 2 is stored as a next fetch point (NFP).

As shown in Fig. 3 and Fig. 5, if routine 1 through 3 are successively carried out, they can be stored in the address trace cache 220 by the above-mentioned manner, respectively. If routines 1 through 3 are not repeatedly carried out, the address of each instruction composing routines 1 through 3 is sequentially written therein. When branch prediction is missed, the loop counter is recomposed with the latest updated loop count value.

Referring now to Fig. 6, if, for example, a routine 1 shown in Fig. 3 is stored in the address trace cache 220, an address of an initially executed instruction A is stored into a start address of routine 1 while an address of a finally executed instruction B is stored into

an end address thereof. Since total repetition times of the routine 1 is 30, an old access loop counter is stored as 30. Whenever routine 1 is repeatedly carried out, a value of a current access loop counter increases by 1. In the same manner, information of routines 2 and 3 is stored in the address cache 220.

As shown in Fig. 6, since the address cache 220 is composed of an address where each routine is started, an address where each routine is finished, a current access loop counter, and an old access loop counter, only four data storing areas are required to store information of a repeated routine. Therefore, total 12 data storing areas are required to store routines 1 through 3 in the address trace cache 220. In this case, if 32 bits are utilized to store each piece of information, a total of 384 bits (i.e., 48 bytes) are required to store routines 1 through 3. This is smaller by about 16.7 times than a data storing area utilized in a conventional trace cache.

Such an effect may be significant, as the number of repeated instructions in a routine becomes large or the number of repetitions of instructions rises. A trace cache of this invention utilizes a data storing area that is considerably reduced in comparison with a conventional trace cache, resulting in decreased chip size and manufacturing unit price. Moreover, the trace cache stores an address trace itself to each instruction with a decoded form, reducing an address decoding time of the instruction.

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

1. A branch prediction method using a trace cache comprising the steps of:

if a routine composed of unrepeated instruction is to be executed, storing an address corresponding to each instruction in the trace cache according to an order of executed instructions; and

if a routine composed of repeated instructions is to be executed, storing a routine start address, a routine end address, current access times of the routine, and total access times of the routine.

2. The method of Claim 1, wherein the trace cache includes loop counters for counting the current access times and the total access times, if the routine composed of repeated instructions is carried out.

3. The method of Claim 2, further comprising addressing a start address which will be subsequent to the routine, if values of the loop counters are identical to each other.

4. The method of Claim 2, further comprising recomposing the loop counter if branch prediction is missed, wherein the loop counter utilizes the latest updated loop count value.

BRANCH PREDICTION METHOD USING ADDRESS TRACE

Abstract of the Disclosure

A branch prediction method using an address trace is described. An address trace corresponding to an executed instruction is stored itself with a decoded form. After appointing a start address and an end address of a repeated routine, current routine accessing times and total accessing times are compared with each other, confirming the end of the routine and storing address information of the next routine. Therefore, access information of the repeated routine can be stored using a small amount of a trace cache.

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Fig. 1

(a)

(b)

(c)

(d)

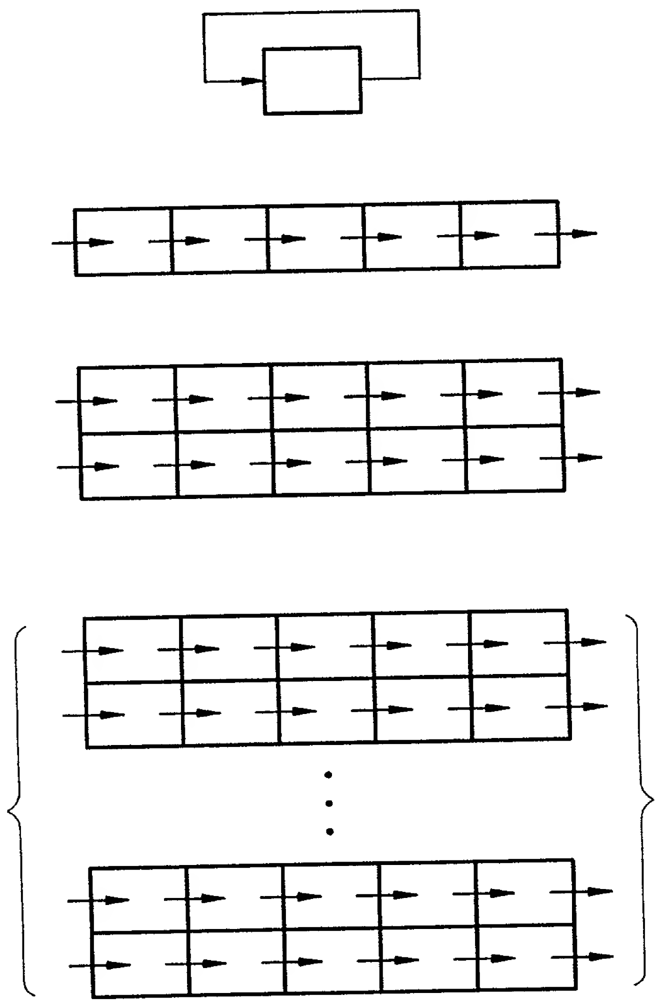


Fig. 2A

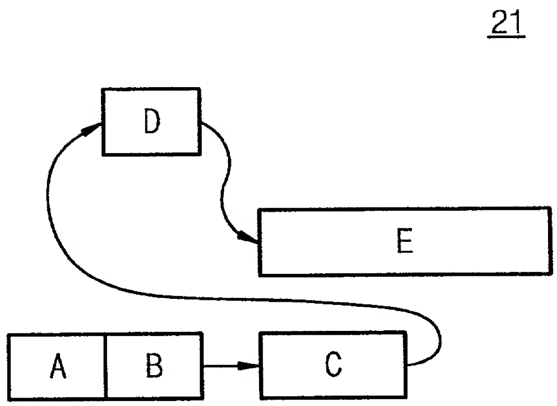


Fig. 2B

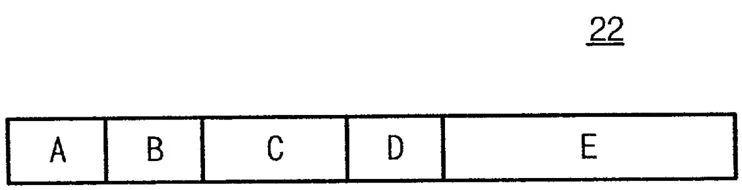


Fig. 3

```
for (i=1 ; i≤30 ; i++)
{
      Operation A ;
      Operation B ;
}
```

Routine 1

```
for (j=1 ; j≤20 ; j++)
{
      Operation C ;
      Operation D ;
      Operation E ;
}
```

Routine 2

```
for (k=1 ; k≤40 ; k++)
{
      Operation F ;
      Operation G ;
}
```

Routine 3

Fig. 4

(Prior Art)

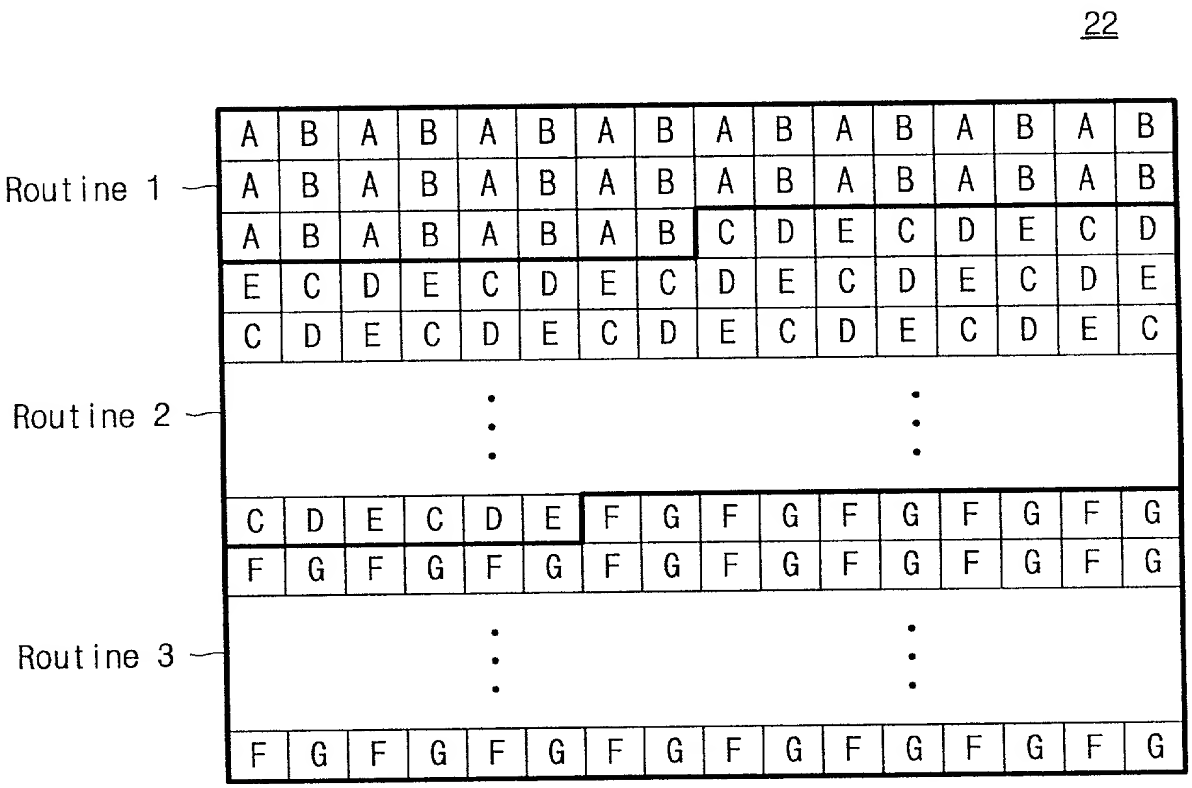


Fig. 5

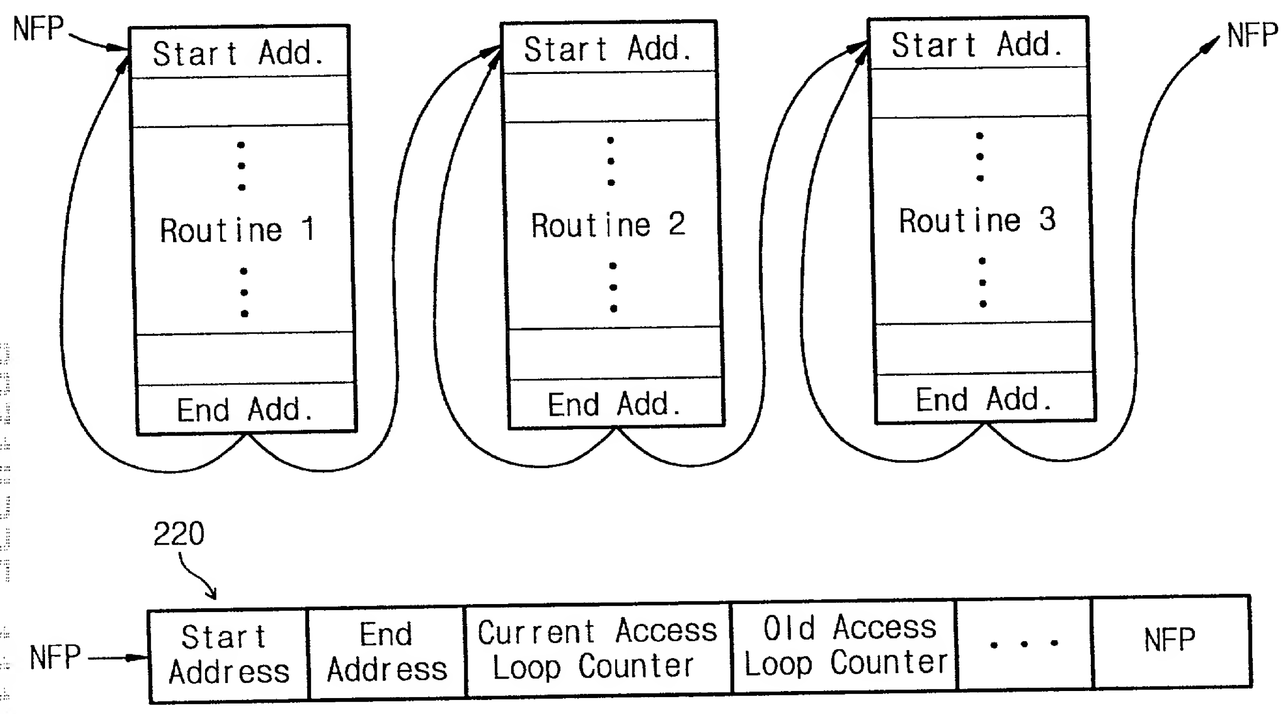
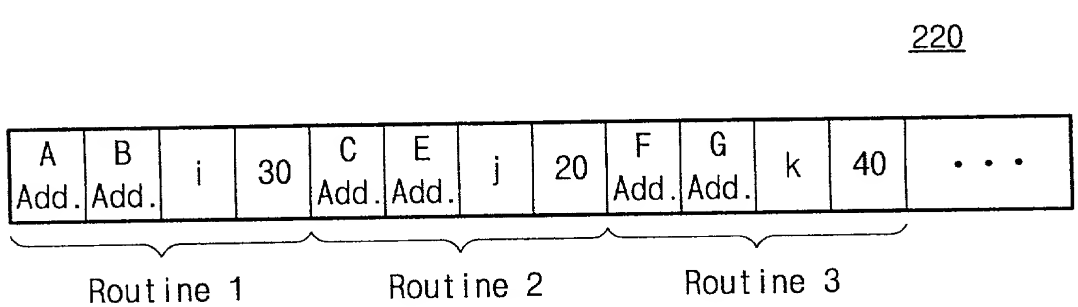

NFP
Start Add.
Routine 1
End Add.
Start Add.
Routine 2
End Add.
Start Add.
Routine 3
End Add.
NFP
220
NFP
Start Address
End Address
Current Access Loop Counter
Old Access Loop Counter
. . .
NFP

Fig. 6


220
A Add.
B Add.
i
30
C Add.
E Add.
j
20
F Add.
G Add.
k
40
. . .
Routine 1
Routine 2
Routine 3

DECLARATION, PETITION AND POWER OF ATTORNEY FOR PATENT APPLICATION	Attorney Docket No: SAM-169

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Branch Prediction Method Using Address Trace

the specification of which (check only one):

_X_ is attached hereto.

____ was filed as United States Patent Application

Serial No. ____________

on ____________

and was amended

on ____________.

(if applicable)

____ Was filed as PCT Patent Application

Serial No. ____________

on ____________

and was amended under PCT Article 19

on ____________.

(if applicable)

I hereby state that I have reviewed and understand the contents of the specification, including the claims as amended by any amendment referred to herein.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119:

COUNTRY (if PCT indicate PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. § 119 (YES/NO)
Republic of Korea	99-50627	13 November 1999	YES

K:\[illegible]

DECLARATION, PETITION AND POWER OF ATTORNEY FOR PATENT APPLICATION	Attorney Docket No: **SAM-169**

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

PRIOR U.S. APPLICATIONS FOR BENEFIT UNDER 35 U.S.C. § 119(e):

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATION(S) DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. § 120:

APPLICATION NUMBER (If PCT indicate PCT)	DATE OF FILING (day, month, year)	STATUS: (PATENTED, PENDING OR ABANDONED)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Maurice E. Gauthier	Reg. No. 20,798	Patrick J. O'Shea	Reg. No. 35,305
Richard L. Stevens	Reg. No. 24,445	Arlene J. Powers	Reg. No. 35,985
Matthew E. Connors	Reg. No. 33,298	Steven M. Mills	Reg. No. 36,610
William E. Hilton	Reg. No. 35,192	Anthony P. Onello, Jr.	Reg. No. 38,572

Send Correspondence to:	Direct Telephone Calls to:
Steven M. Mills, Esq. Samuels, Gauthier & Stevens LLP 225 Franklin Street Boston, Massachusetts 02110	Steven M. Mills, Esq. (617) 426 9180 Ext. 140 (617) 426-2275 (facsimile)

Wherefore I petition that letters patent be granted to me for the invention or discovery described and claimed in the attached specification and claims, and hereby subscribe my name to said specification and claims and to the foregoing declaration, power of attorney, and this petition.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signature		Date	Nov. 15, 2000
Full Name of 1st Inventor	Family Name Park	First Given Name Sung-Bae	Second Given Name
Residence & Citizenship	City Kyunggi-do	State or Foreign Country Republic of Korea	Country of Citizenship Republic of Korea
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